US005970255A

United States Patent [19]

Tran et al.

[11] Patent Number: 5,970,255

[45] Date of Patent: Oct. 19, 1999

[54] **SYSTEM FOR COUPLING PROGRAMMABLE LOGIC DEVICE TO EXTERNAL CIRCUITRY WHICH SELECTS A LOGIC STANDARD AND USES BUFFERS TO MODIFY OUTPUT AND INPUT SIGNALS ACCORDINGLY**

[75] Inventors: **Nghia Tran**, San Jose; **Ying Xuan Li**, Santa Clara; **Janusz Balicki**; **John Costello**, both of San Jose, all of Calif.

[73] Assignee: **Altera Corporation**, San Jose, Calif.

[21] Appl. No.: **08/543,649**

[22] Filed: **Oct. 16, 1995**

[51] **Int. Cl.**[6] **G06F 13/10**

[52] **U.S. Cl.** **395/893**; 395/828; 395/830; 395/834; 395/882; 395/884

[58] **Field of Search** 326/44, 71, 75, 326/81, 83, 108, 38, 41, 73, 86; 365/229, 185.14; 340/825.8; 380/3; 395/569, 828, 830, 834, 882, 884, 893; 327/333; 375/377; 711/103, 104

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 34,444	11/1993	Kaplinsky	340/825.8
4,032,800	6/1977	Droscher et al.	326/81
4,609,986	9/1986	Hartmann et al.	364/20 C
4,617,479	10/1986	Hartmann et al.	307/465
4,677,318	6/1987	Veenstra	307/465
4,713,792	12/1987	Hartmann et al.	364/900
4,774,421	9/1988	Hartmann et al.	307/465
4,871,930	10/1989	Wong et al.	307/465
4,899,067	2/1990	So et al.	307/465
4,912,342	3/1990	Wong et al.	307/465
4,972,470	11/1990	Farago	380/3
4,975,602	12/1990	Nhu	326/71
4,987,578	1/1991	Akins et al.	375/377
4,994,691	2/1991	Naghshineh	326/78
5,003,200	3/1991	Sakamoto	307/465
5,023,488	6/1991	Gunning	307/475
5,101,122	3/1992	Shinonara	326/44
5,121,006	6/1992	Pedersen	307/465
5,121,359	6/1992	Steele	365/229
5,220,214	6/1993	Pedersen	307/465
5,235,219	8/1993	Cooperman et al.	326/83
5,260,610	11/1993	Pedersen et al.	307/465
5,260,611	11/1993	Cliff et al.	307/465
5,350,954	9/1994	Patel	307/465
5,371,422	12/1994	Patel et al.	326/41
5,374,858	12/1994	Elmer	327/333
5,412,599	5/1995	Daniele et al.	365/185
5,426,744	6/1995	Sawase et al.	395/569
5,428,305	6/1995	Wong et al.	326/75
5,483,178	1/1996	Costello et al.	326/41
5,534,798	7/1996	Phillips et al.	326/108
5,590,305	12/1996	Terrill et al.	395/430
5,600,267	2/1997	Wong et al.	326/73
5,732,407	3/1998	Mason et al.	711/104

OTHER PUBLICATIONS

R.C. Minnick, "A Survey of Microcellular Research," Journal of the Association for Computing Machinery, vol. 14, No. 2, pp. 203–241, Apr. 1967.

S.E. Wahlstrom, "Programmable Logic Arrays—Cheaper by the Millions," Electronics, Dec. 11, 1967, pp. 90–95.

Recent Developments in Switching Theory, A. Mukhopadhyay, ed., Academic Press, New York, 1971, chapters VI and IX, pp. 229–254 and 369–422.

Primary Examiner—Thomas C. Lee

Assistant Examiner—Chien Yuan

Attorney, Agent, or Firm—Fish & Neave; Robert W. Morris; Michael F. Shanahan

[57] **ABSTRACT**

A programmable input/output device for use with a programmable logic device (PLD) is presented comprising an input buffer, an output buffer and programmable elements. The programmable elements may be programmed to select a logic standard for the input/output device to operate at. For instance, a given set of Select Bits applied to the programmable elements may select TTL logic, in which case the input and output buffers would operate according to the voltage levels appropriate for TTL logic (e.g., 0.4 volts to 2.4 volts). For a different set of Select Bits, the GTL logic standard would be applied (e.g., 0.8 volts to 1.2 volts). The invention enables a single PLD to be used in conjunction with various types of external circuitry.

34 Claims, 5 Drawing Sheets